Formalization of Reliable Digital Circuits

Using B method and VHDL

HEUDIASYC
Univ. Compiègne
Jean-Louis Boulanger

LIFL
Univ. Lille I
Ammar Aljer
Philippe Devienne
Sophie Tison

National Laboratory
of Transports and
Security Research
Georges Mariano

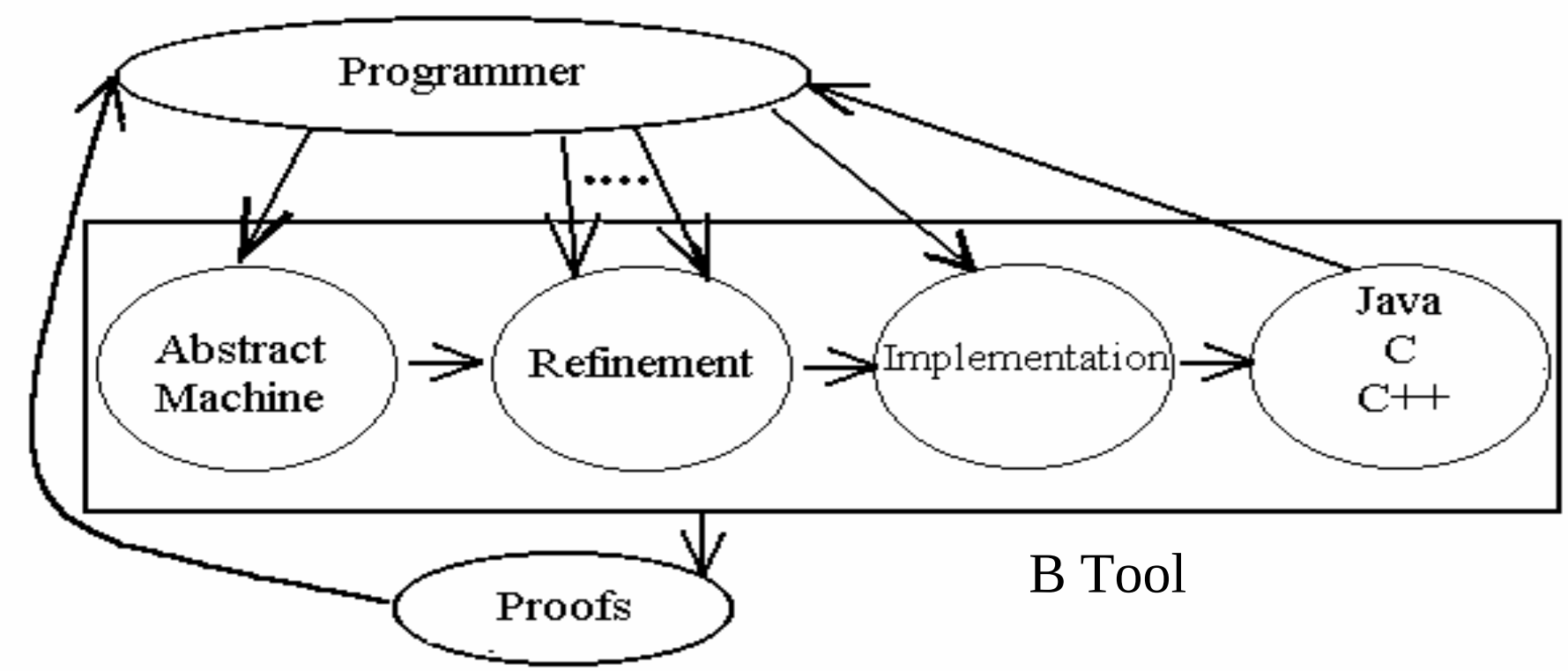
B Method

Mathematical tools (set theory, logic) : to specify and implement a model.

Refinement : Abstract machine $\longrightarrow^{*}$ Implementation

Specification $\Rightarrow$ Deterministic computation

Proofs : automatically generated by Atelier B (FR) & B_Toolkit (UK)



Circuits Design ⇔ B Method

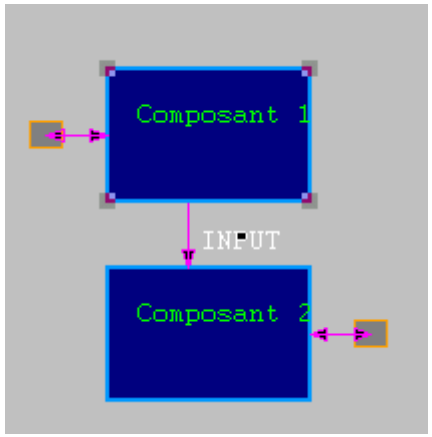
Functional Specification	Abstract Machine
Operational Spec. + components	Refinement
Validation	Theorem Proving

VHDL : Very high speed circuits Hardware Design Language

VGUI (Graphical Interface)

ANTLR

(Parser)



VHDL

B Method

Entity + Architecture

Conclusion

Features

- Translation at a high level preserving modularity and hierarchy ($\Leftrightarrow$?)
- VHDL Modules with initialization and invariant properties (logic formulas)
- Top-down approach for design of digital circuits with pre-verification
- Validation of properties described by logic formulas
- Embedded systems with mixed software and hardware components

Limits

- Interactive proofs
- Real Time
- Large scale circuit